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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, KOU YI	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,212	NAYAK ET AL.	
	Examiner	Art Unit	
	Kou-Yi K. Chen	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 21-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 21-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on January 7, 2002.

2. Per Applicants' request claims 2-20 and 40-52 have been cancelled.

3. Claims 1, and 21-39 are pending in the application.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 1 is rejected under 35 U.S.C. § 101 as being directed to nonstatutory subject matter.

Claim 1 recites: "specifying at least one resource or functionality using at least one construct in a Resource Description Language (RDL) wherein at least one component or function is specifiable for processing by a high-level synthesis compiler". The language of the claim raises a question as to whether the claim is directed merely to an abstract idea which does not result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 USC § 101. In order for the claimed method to produce a "useful, concrete, and tangible" result, a direct recitation of a practical application is suggested.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 1 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. A single step claim, i.e., where a step recitation does not appear in combination with another recited element of step, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single step claim which covered every conceivable step for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those step known to the inventor.). When claims depend on a recited property, a fact situation comparable to Hyatt is possible, where the claim covers every conceivable structure (step) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, and 21-39 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,170,464 to Hayes et al. (hereinafter, "Hayes").

As per claim 1

Hayes teaches:

A computer-automated method for electronic design specification ("Handel-C allows one to use a high-level language to program FPGAs " in [0145] lines 1-2, and "Handel-C is thus designed to enable the compilation of programs into synchronous hardware; it is aimed at compiling high level algorithms directly into gate level hardware" in [0163] lines 1-4) comprising the step of:

specifying at least one resource or functionality using at least one construct in a Resource Description Language (RDL) ("A program may be written in Handel-C to generate all required state machines, while one can specify storage requirements down to the bit level" in [0145] lines 6-9, wherein Handel-C is a Resource Description Language, also see FIG. 84 for Handel-C Statements such as par{...} meaning Parallel composition, and seq{...} for Sequential execution, etc.) wherein at least one

component or function is specifiable for processing by a high-level synthesis compiler ("The compiler compiles and optimizes Handel-C source code into a file suitable for simulation or a net list which can be placed and routed on a real FPGA" in [0163] lines 12-14).

Claims 2-20 (Cancelled)

As per claim 21, the rejection of claim 1 is incorporated, and further, Hayes teaches: a resource is used to specify an architecture and a plurality of functionalities ("The present invention relates to programmable hardware architectures and more particularly to programming field programmable gate arrays (FPGA's)" in [0001] lines 1-3).

As per claim 22, the rejection of claim 1 is incorporated, and further, Hayes teaches: a unit is used to specify a hardware structure comprising a hierarchical representation of one or more hardware structure ("Handel-C includes a multiplication operator as part of the language, this example serves as a starting point for generating large regular hardware structures using macros" in [4274] lines 5-8).

As per claim 23, the rejection of claim 1 is incorporated, and further, Hayes teaches: A UNITDEF value defines or describes a hierarchy of a unit (see FIG. 6 "a core": "A discrete piece of code, compiled to a specific architecture, that may be used as part of a larger design").

As per claim 24, the rejection of claim 1 is incorporated, and further, Hayes teaches: a RESOURCEDEF value defines a resource among a set of functionality or associated property (see FIG. 53 for various resource definitions, such as ram, register, rom, and signal, etc.).

As per claim 25, the rejection of claim 1 is incorporated, and further, Hayes teaches: a RCONNECT value denotes a connection between an origin resource and a destination resource via connecting resource (see FIG. 56 "extpath": "specify any direct logic (combination logic) connections to another port").

As per claim 26, the rejection of claim 1 is incorporated, and further, Hayes teaches: a USES value indicates one or more resource used by a particular resource, the USES value defining at least one virtual resource for building at least one physical resource in an architecture ("Selecting the Symbol View tab 1302 of the workspace window then shows icons 1304 representing logic and architectural variables, functions and procedures" in [0350] lines 10-12).

As per claim 27, the rejection of claim 1 is incorporated, and further, Hayes teaches: a FUNCTIONALITY value specifies a set of one or more basic operator to provide functionality (see FIG. 85A for all Operators and their meanings).

As per claim 28, the rejection of claim 1 is incorporated, and further, Hayes teaches: a FUNCTIONALITYDEF value defines a composition of a new functionality ("Handel-C also has functions, variables and expressions similar to conventional C. There are restrictions where operations are not appropriate to hardware implementation and extensions where hardware implementation allows additional functionality" in [2797] lines 1-5).

As per claim 29, the rejection of claim 1 is incorporated, and further, Hayes teaches: a DCONNECT value connects a plurality of basic operators while constructing a new functionality ("A Handel-C macro library may be used for bit manipulation and arithmetic operations" in [0145] lines 11-12).

As per claim 30, the rejection of claim 1 is incorporated, and further, Hayes teaches: an INPUT value specifies one or more node for constructing a new functionality (see FIG. 84 "Channel ? Variable; Channel input").

As per claim 31, the rejection of claim 1 is incorporated, and further, Hayes teaches: an OUTPUT value specifies one or more output node for constructing a new functionality (see FIG. 84 "Channel ! Expression; Channel output").

As per claim 32, the rejection of claim 1 is incorporated, and further, Hayes teaches:

an OPT_INPUT value specifies one or more optional input node while constructing a new functionality (see FIG. 84 "ifselect (Expression [{...} else {...}] Conditional compilation".

As per claim 33, the rejection of claim 1 is incorporated, and further, Hayes teaches: an if value (see FIG. 84 "if (Expression) [{...} else {...}]") specifies an arbitrarily complex connection between a plurality of resources in conjunction with using a for value (see FIG.84 "for (Init ; Test ; Iter) {...}").

As per claim 34, the rejection of claim 1 is incorporated, and further, Hayes teaches: a for value specifies an arbitrarily complex connection between a plurality of resources in an architecture (see FIG.84 "for (Init ; Test ; Iter) {...}").

As per claim 35, the rejection of claim 1 is incorporated, and further, Hayes teaches: at least one operator in a resource design language (RDL) specifies a hardware and a processing of the hardware ("The present invention relates to programmable hardware architectures and more particularly to programming field programmable gate arrays (FPGA's)" in [0001] lines 1-3).

As per claim 36, the rejection of claim 32 is incorporated, and further, Hayes teaches: a hierarchy traversal operator (->) specifies a unit or resource embedded within one or more units by specifying a chain of units hierarchically with the -> operator denoting a

child-parent relationship in a hierarchy ("The structure pointer operator (->) can be used, as in ISO-C" in [3744] lines 3-4).

As per claim 37, the rejection of claim 32 is incorporated, and further, Hayes teaches: an array operator ([ ]) specifies an array or collection of one or more resource or unit (see FIG. 86A "[ ] array index delimiters").

As per claim 38, the rejection of claim 32 is incorporated, and further, Hayes teaches: a comment operator (//) inserts one or more comment in an architecture file ("Handel-C also provides the C++ style // comment marker which tells the compiler to ignore everything up to the next newline" in [2817] lines 1-3).

As per claim 39, the rejection of claim 32 is incorporated, and further, Hayes teaches: operators +, -, *, /, %, =, !=, >, >=, <, and <= comprise a set of arithmetic or logical operators for constructing one or more expression for use with an if construct selectively to make one or more connection in a for loop (see FIG. 84 and FIG. 86B).

Claim s40-52 (Cancelled)

Conclusion

10. The prior art made of record, and not relied upon, is considered pertinent to applicant's disclosure.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kou-Yi K. Chen** whose telephone number is **571-272-8592**. The examiner can normally be reached **from 8:30 am to 5:00 pm on M-F**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on 571-272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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